Molybdenum Disulfide Nanoflake–Zinc Oxide Nanowire Hybrid Photoinverter

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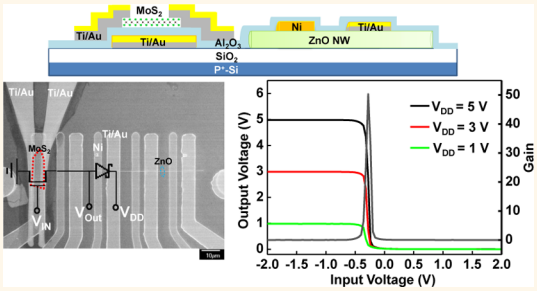
ABSTRACT We demonstrate a hybrid inverter-type nanodevice composed of a MoS_2 nanoflake field-effect transistor (FET) and ZnO nanowire Schottky diode on one substrate, aiming at a one-dimensional (1D)–two-dimensional (2D) hybrid integrated electronic circuit with multifunctional capacities of low power consumption, high gain, and photodetection. In the present work, we used a nanotransfer printing method using polydimethylsiloxane for the fabrication of patterned bottom-gate MoS_2 nanoflake FETs, so that they could be placed near the ZnO nanowire Schottky diodes that were initially fabricated. The ZnO nanowire Schottky diode and MoS_2 FET worked respectively as load and driver for a logic inverter, which exhibits a high voltage gain of ~50 at a supply voltage of 5 V and also shows a low power consumption of less than 50 nW. Moreover, our inverter effectively operates as a photoinverter, detecting visible photons, since MoS_2 FETs appear very photosensitive, while the serially connected ZnO nanowire Schottky diode was blind to visible light. Our 1D–2D hybrid nanoinverter would be quite promising for both logic and photosensing applications due to its performance and simple device configuration as well.



KEYWORDS: MoS_2 nanoflake FET · ZnO nanowire · photoinverter · Schottky diode · power consumption · nanotransfer printing

Two-dimensional (2D) materials are extremely interesting as building blocks of next-generation nanoelectronic devices because of their promising properties. The most widely studied two-dimensional material to date is graphene due to its high carrier mobility (μ) over 100 000 $cm^2/V \cdot s$,[1,2] but it has considerable limitations in regard to real device applications. In untreated form, graphene has no band gap, resulting in small current on/off ratios in field-effect transistors; graphene could hardly be used for switching circuits.[3,4] As one alternative 2D material beyond graphene, the molybdenum disulfide (MoS_2) chalcogenide nanoflake recently appeared, circumventing the drawbacks of graphene (although its practical mobility is limited to a few hundred $cm^2/V \cdot s$).[5,6] Bulk MoS_2 is known to have an indirect band gap of ~1.2 eV, although the few-angstrom-thin single-layered MoS_2 has been reported to exhibit a direct band gap of 1.8 eV.[6–11] The MoS_2 nanoflake has thus been investigated for field-effect transistors (FETs), photodetectors, and even logic circuits for NAND, NOR, small signal amplifiers, and ring oscillators.[6,9,12–17] However, good practical circuits using more than two MoS_2-based FETs generally need electron beam (e-beam) lithography for fabrication, since the nanoflakes of 2D MoS_2 are not large enough to pattern by photolithography. Therefore, 2D MoS_2-based circuits are not that easy to realize by conventional photolithography on one substrate. Hence, a more favorable and simple way to use a MoS_2-based device may be necessary.

Here, we report a bottom-up fabrication approach that uses quite a conventional method, to integrate different nanoscale building blocks for practical device applications. A MoS_2 nanoflake FET and a ZnO nanowire Schottky diode were coupled in series on the same substrate, to form an electric and photoelectric hybrid inverter. In fact, similar types of devices were very recently reported for a complementary inverter and gate-tunable p–n diode adopting MoS_2 and carbon nanotubes (CNTs),[18,19] but the incorporation of a ZnO nanowire device to a MoS_2 FET has not been reported yet. Such hybrid nanodevices would be novel because of their multifunctionalities; the properties of MoS_2 nanoflakes are different from those of ZnO nanowires, but

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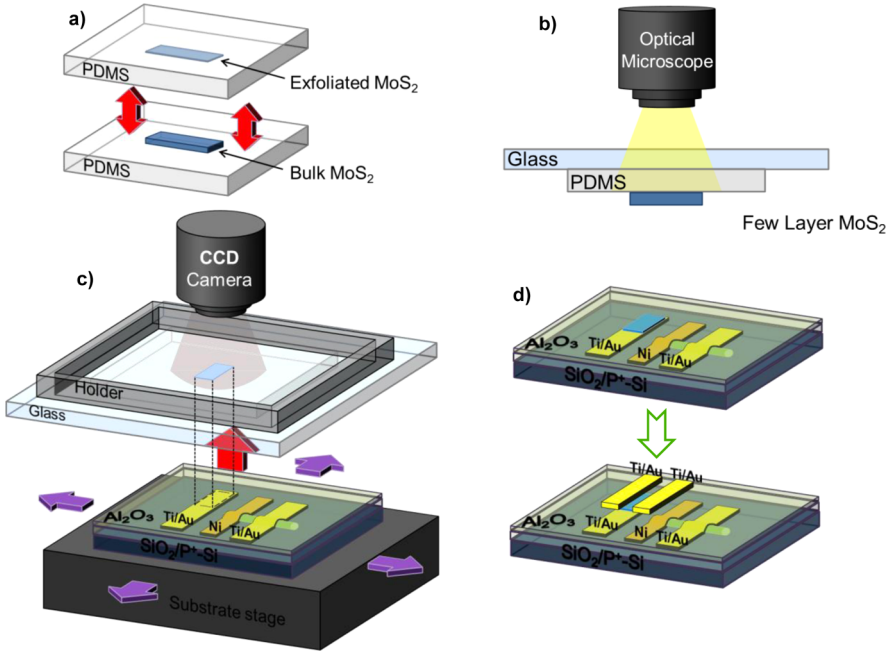

Figure 1. Schematics of the direct imprint (nanotransfer printing) process for the MoS_2 nanoflake FET–ZnO nanowire Schottky diode inverter: (a) MoS_2 exfoliation by PDMS, (b) selection of an optimally thin MoS_2 flake by utilizing a microscope, (c) nanotransfer printing of the chosen MoS_2 flake on the target site near the already fabricated ZnO nanowire diode, and (d) 3D view of the MoS_2 device placed near the ZnO nanowire Schottky diode; top contact Ti/Au forms the MoS_2 nanoflake FET, which will be connected to a Ni Schottky contact of the ZnO nanowire diode, so that finally an inverter forms on the same substrate.

both would be compensating each other. In the present study, we used such different but compensating properties to realize an electrical and photodetecting inverter. For a logic inverter, we used the MoS_2 FET for a high-speed switch, while the ZnO Schottky diode was used as a resistor for low power consumption or high voltage inverter gain. For a visible photodetecting inverter, a MoS_2 FET acts as a photosensitive switch due to the visible light-matching band gap of MoS_2, while a ZnO nanowire Schottky diode acts as photoblind resistor. For hybrid device processes, we developed a direct imprint (or nanotransfer printing) process and also utilized conventional photolithography, to place the MoS_2 flake near the ZnO nanowire as shown in Figure 1a–d. As a result, our inverter has been nicely fabricated as shown in Figure 2a–c, demonstrating a high voltage gain of ~50 and a low power consumption of 50 nW and also exhibiting good dynamic photoresponses in the visible range. More fabrication details involved with Figures 1 and 2 are found in the Methods section.

RESULTS AND DISCUSSION

Figure 3a shows the linear and logarithmic scale current–voltage (I–V) characteristics of the ZnO nanowire Schottky diode, where 1 μA is observed as on-current at 3 V forward bias voltage. The ON/OFF current ratio is more than 100, while the ideality factor, η, of the diode is estimated to be 1.25. Figure 3b shows the drain current–gate voltage (I_D–V_G) transfer curve of the bottom-gate MoS_2 nanoflake FET at a drain–source voltage, V_D, of 0.1 V, where I_D of more than 1 μA is obtained along with an ON/OFF current ratio of ~10^5 and subthreshold slope (SS) of ~0.145 V/dec. The thickness of the MoS_2 flake is ~32 nm, as shown in the atomic force microscope data of Figure 3c. Our MoS_2 device has a gate hysteresis of less than 2 V, and its linear mobility, μ, is around 6 $cm^2/V\cdot s$, as shown in the inset of Figure 3b, while the mobility estimation came from a well-known equation, $\mu = (\partial I_D/\partial V_G)$-$(1/(C_{ox}V_D(W/L)))$, where C_{OX} is the dielectric capacitance (~220 nF/cm^2) and W and L are the channel width and length, respectively (Table S1). The output curve (I_D–V_D) of Figure 3d shows an almost linear characteristic at high drain–source voltage, which indicates a good ohmic contact between Ti/Au and MoS_2 without any thermal annealing. As shown in Supporting Information Figure S1 and Table S1, we could also fabricate another bottom-gate MoS_2 FET with thinner (~25 nm) and thicker (~72 nm) MoS_2 flakes, using the same nanotransfer printing method and 30 nm thin ALD Al_2O_3 for the dielectric layer. In those cases, a higher linear mobility of ~22 $cm^2/V\cdot s$ was achieved from the thinner MoS_2, while a lower mobility of ~4 $cm^2/V\cdot s$ was obtained from the thicker channel. Compared to the previous reports for high mobility over 100 $cm^2/V\cdot s$, our MoS_2 FETs showed relatively lower values than those reported,[6,14,16,20] because our nanoflakes were much thicker than those (a few layer; 0.7–2.0 nm) with top-gate structure[6,16,20]

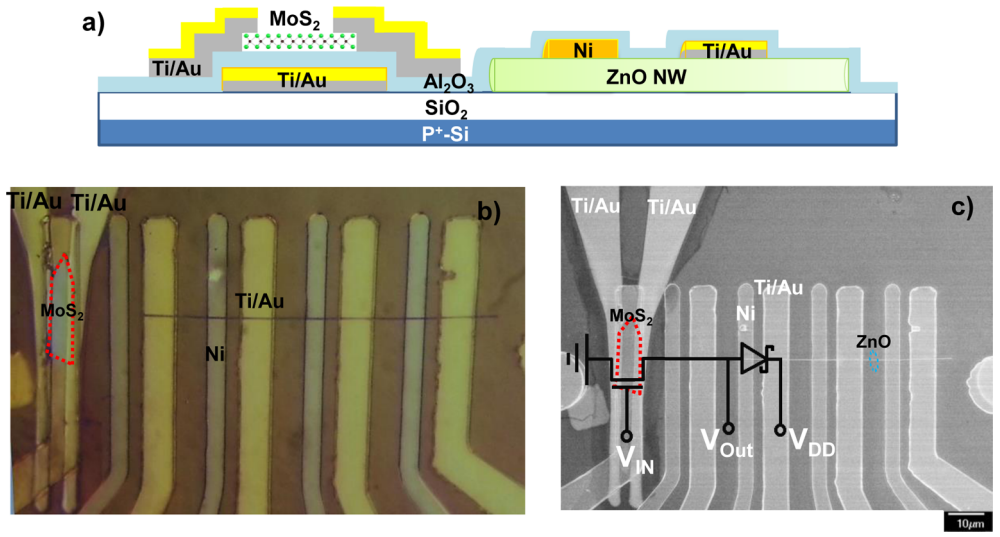

Figure 2. MoS_2 nanoflake FET–ZnO nanowire diode coupled inverter: (a) schematic cross section of the inverter, (b) top-view optical microscopic image, and (c) HRSEM view of the inverter along with the circuit diagram of the FET and Schottky diode drawn over it. V_{DD}, V_{IN}, and V_{OUT} respectively represent supply, input, and output voltages. Al wire bonding was used to connect the two individual devices on the same substrate.

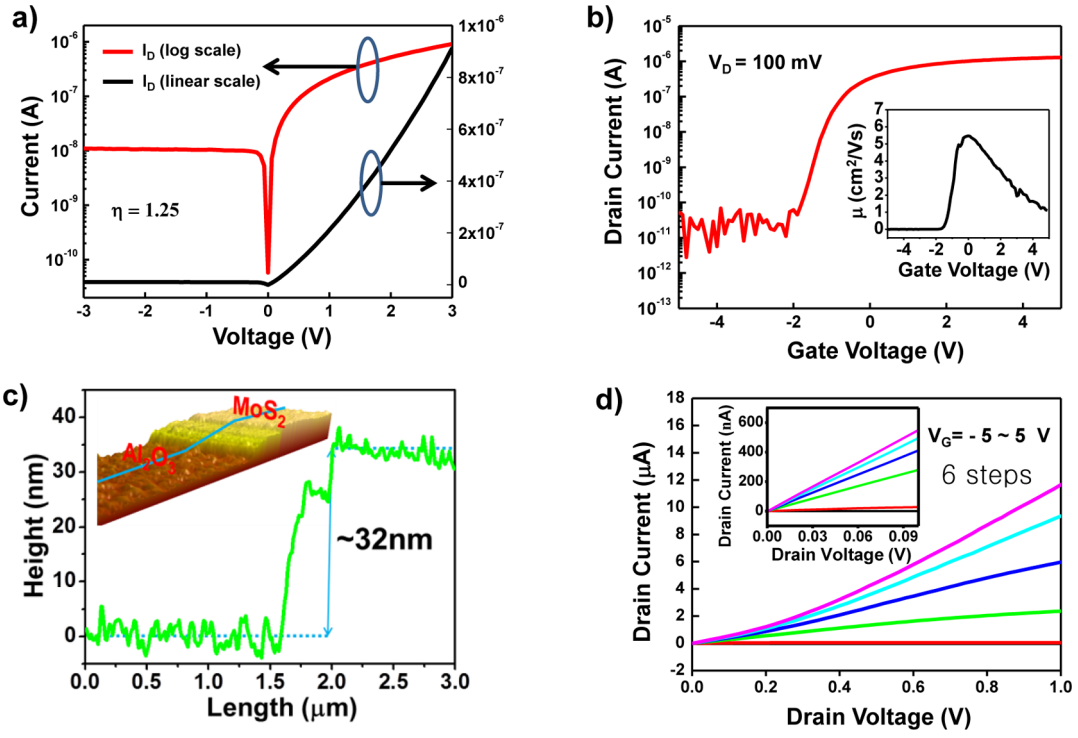

Figure 3. (a) Linear and logarithm scale $I-V$ plots of Ni/ZnO nanowire Schottky diode. (b) Transfer curve of our bottom-gate patterned MoS_2 nanoflake FET and V_G-dependent linear mobility plot (inset). (c) AFM line profile of the MoS_2 flake showing thickness with inset indicating a portion of the flake above Al_2O_3. (d) Output curves of MoS_2 nanoflake FET with inset showing the magnified low-bias linear behavior.

and also because our source–drain metal electrode (Ti/Au) would not be the best-optimized contact.[21,22] Almost the same amount of gate hysteresis was found from those nanoflake FETs, and the cause of such hysteresis is attributed to the surface charge state of back-channel MoS_2, which might be changed by gate bias sweep.[23] It is interesting that the mobility and ON current I_D of FETs decrease with thickness of MoS_2. This is probably because of the parasitic resistance originating from the thickness path of current, which should exist in the device architecture of the top source/drain contact bottom-gate FET as reported in conventional thin-film transistor studies.[21,24,25]

Figure 4a shows the voltage transfer curves (VTCs) of an electrical inverter formed by connecting the MoS_2 nanoflake FET and ZnO Schottky diode in series; the

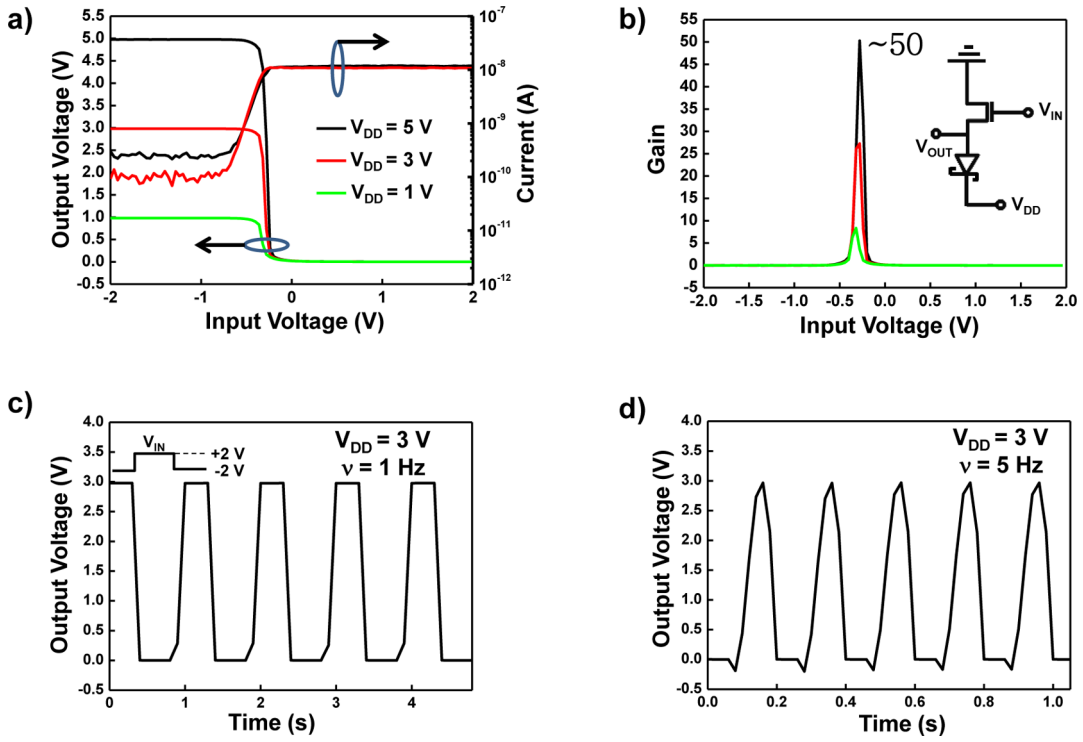

Figure 4. (a) VTCs of our ZnO nanowire−MoS_2 nanoflake-based hybrid inverter obtained at a V_{DD} of 1, 3, and 5 V; I_{DD} curves were also obtained at 3 and 5 V. (b) Corresponding voltage gains (= $-dV_{OUT}/dV_{IN}$) of the inverter and its gate dynamics are observed under a V_{DD} of 3 V by a time domain V_{IN} pulse at (c) 1 and (d) 5 Hz; rising/falling time was as large as ~50 ms, which is probably due to the intrinsic RC delay generated in our unoptimized device archetecture with large parasitic capacitances.

inverter operation was implemented by sweeping the gate-source voltage, V_G (=V_{IN}, the input voltage of the driver in Figure 2c). The transition voltage for high and low states in VTCs appears to be ~-0.5 V, since the turn on voltage of our nanoflake FET was around −1 V (Figure 3b). When three different supply voltages (V_{DD} = 1, 3, and 5 V) are applied, the ZnO diode of our hybrid inverter should be under reverse bias conditions according to the inverter circuit of Figure 2c, so that the reversed biased Schottky diode limits the inverter current (I_{DD}) to less than 10 nA, which leads to low power consumption, less than few tens of nanowatts depending on applied supply voltage. (Estimated power consumption of 30−50 nW is quite low for a non-CMOS inverter.) According to the voltage gain (= $-dV_{OUT}/dV_{IN}$) plots of Figure 4b, quite high gains of 10, 30, and 50 are exhibited for V_{DD} of 1, 3, and 5 V, respectivly, which is almost the highest gain result for MoS_2-based inverters ever reported until now, based on our limited knowledge.[14,16,26] Such high gain is probably related to the current suppression by a reverse-biased Schottky diode as well. The inverter gate dynamics of our inverter are observed under a V_{DD} of 3 V by a time domain V_{IN} pulse at 1 and 5 Hz as shown in Figure 4c and d (with rising time ~50 ms).

For a photosensing application, we prepared a different set of inverters with a thicker MoS_2 layer (~70 nm; Figure 5b and its inset show the MoS_2 thickness in AFM), which may provide some benefits with higher quantum efficiencies under off-state gate bias, absorbing a higher number of visible photons from respective light-emitting diodes (LEDs; intensity was a few mW cm^{-2}): red (630 nm), green (540 nm), and blue (440 nm). According to *I*−*V* curves of Figure 5a and b, the ZnO nanowire Schottky diode appears quite insensitive to visible light, compared to the photoelectric behavior of the patterned MoS_2 FET, which shows a light-induced threshold voltage shift and large photocurrent in the phototransfer curves. The photoblindness of the ZnO Schottky diode is quite expected, because the band gap of the ZnO nanowire is as high as ~3.2 eV, so that the nanowire mostly transmits visible light with lower energy,[27,28] and also because the light-exposed area of the nanowire is almost out of the electric (*E*)-field and any photoexcited carriers would thus be recombined with their original (trap) sites.[29] However, the patterned MoS_2 FET meets a different situation, since its band gap is around 1.2 eV, which is small enough to receive and absorb visible photons. Excited electrons are easily collected by the drain even at a low V_D of 0.1 V, to contribute to the photosignal particularly under off-state gate bias. These photocurrents are converted to a voltage signal (V_{OUT}) when the two devices—the ZnO nanowire Schottky diode and MoS_2 FET—are coupled in series to form a photoinverter.

The photoinduced behavior is now shown in Figure 5c as VTCs under dark, red, green, blue, and

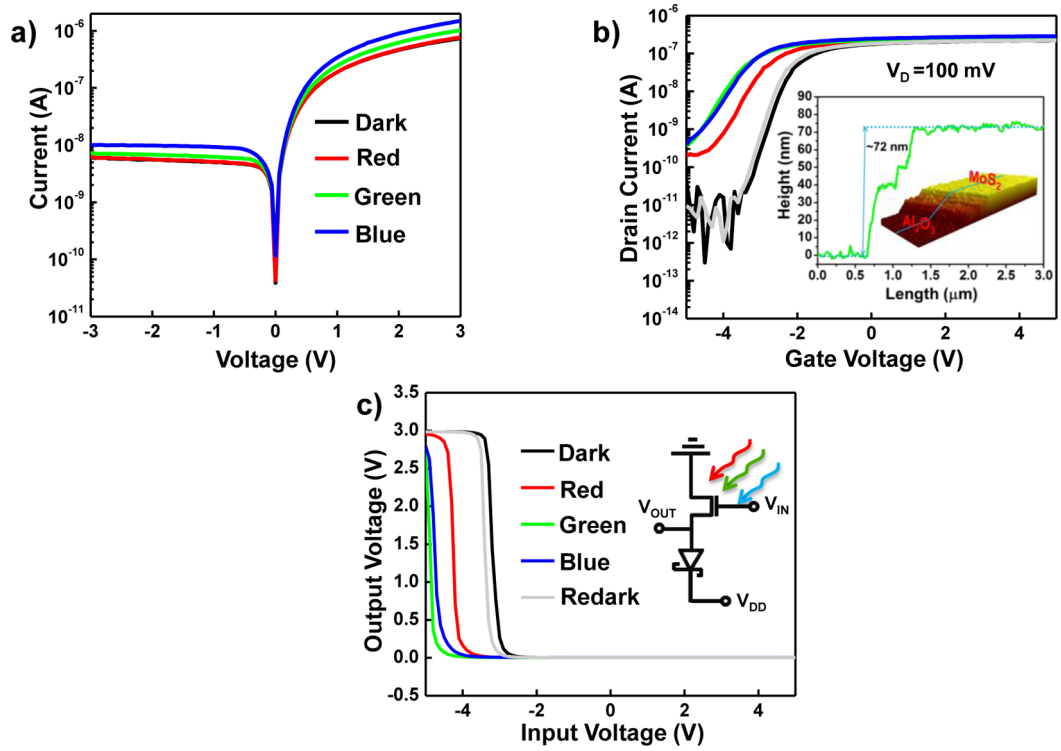

Figure 5. (a) *I*−*V* curves of a ZnO Schottky diode under red (R), green (G), and blue (B) illuminations. (b) Photoinduced transfer curves of a MoS_2 FET with 70 nm thick MoS_2 flake (inset AFM), as obtained under the same R, G, and B illuminations. (c) Photoinduced VTCs of our photoinverter and its circuit (inset).

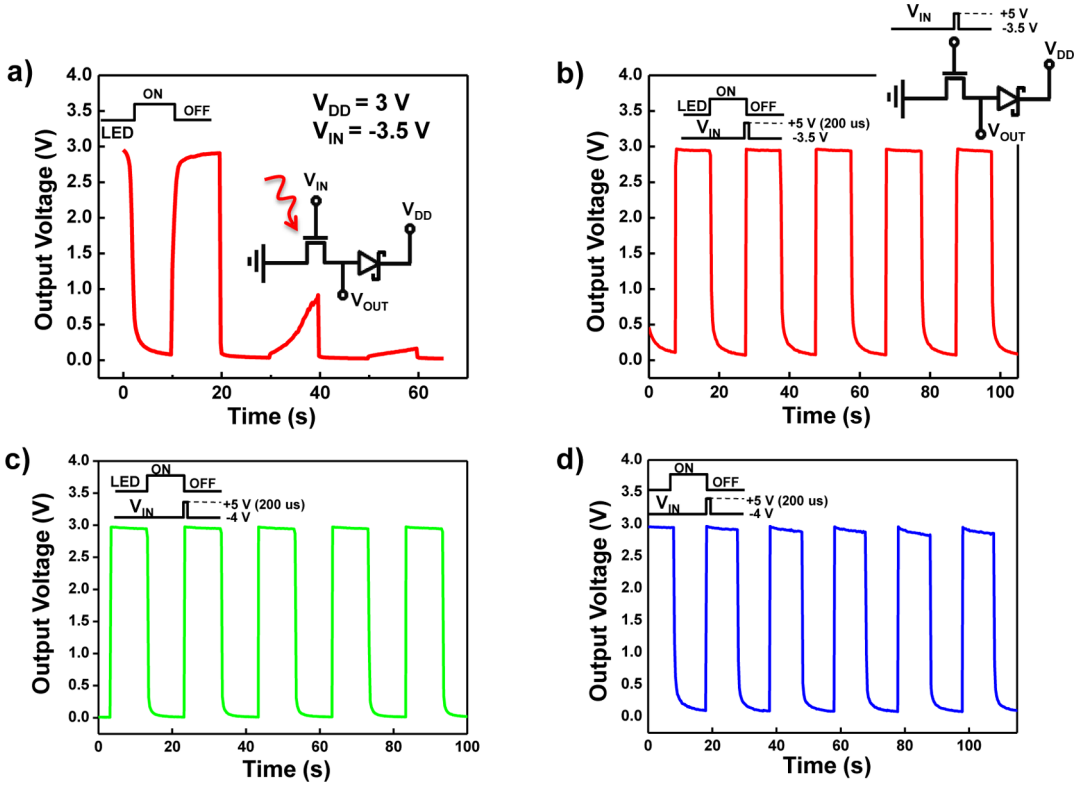

Figure 6. (a) Photoinverter dynamics under periodic illumination of red light (inset schemes and circuit) shows PPC problems in the absence of positive gate pulse. (b, c, d) However, a +5 V gate pulse of 200 μs (inset pulse scheme) removes the PPC issues for red, green, and blue light, respectively.

redark conditions, along with inset inverter circuit (inverter supply voltage (V_{DD}) was fixed at 3 V, and the voltage gain was ~14). As the threshold voltage shift was shown in the transfer curves of Figure 5b, the photoinduced VTC curve shift is observed in Figure 5c as a reflection of the transfer curves. After switching off the illumination, our inverter device mostly recovers its initial dark behavior (the smaller shift induced by red light is probably due to the optical power differences). Since the initial dark−illumination−redark stages were reproducibly repeated in the VTC regime, we attempted a more practical application: photodynamic output voltage (V_{OUT}) recording in a time domain. ON-and-OFF repeating of LED illumination was implemented to record V_{OUT} under a fixed input voltage (V_{IN}) of −3.5, −4, and −4 V (respectively for red, green, and blue), while a supply voltage (V_{DD}) was fixed at 3 V. However, any decent photoinverting dynamic output was not easy to achieve, as shown in Figure 6a for red (and Figure S2 for green and blue); persistent photoconductivity (PPC) phenomena are rather observed. The observed PPC have been explained based on a few different models including random local-potential fluctuation (RLPF) and large lattice relaxation (LLR) models, which are more applicable for 2D layered materials.[13,30−34] In the RLPF model, random local-potential fluctuations induced by compositional fluctuations are responsible for PPC, while in the LLR model the PPC involves photoexcitation of electrons from deep-level-like traps (DX-like centers).[30]

An electron-capture barrier is created by lattice relaxation, preventing recapture/recombination of electrons by these trap centers.[35−38] In the present work, these PPC issues were effectively resolved by using a short accumulation (on-state) voltage pulse (by less than 200 μs short gate pulse), as clearly shown in Figure 6b, c, and d for red, green, and blue illumination. According to the inset pulse schemes in the figures, short positive gate pulses (to +5 V) are instantaneously applied to accumulate electrons at the interface region, immediately after the light exposure. This positive gate pulse process accelerates the recombination process and suppresses the electron-capture barrier. The trap-induced transient I_D may rapidly fall to the initial dark value by the gate pulse, and as a result, our photoinverter shows a short recovery time of less than 0.2 s, ensuring somewhat desirable behavior of the dynamic photodetector.

CONCLUSION

In summary, by using a nanotransfer printing method and conventional lithography, we have conveniently fabricated a 1D−2D hybrid inverter composed of a ZnO nanowire Schottky diode and a MoS_2 nanoflake patterned bottom-gate FET. The ZnO nanowire Schottky diode and MoS_2 FET worked respectively as load and driver for a logic inverter, which exhibits a high voltage gain of ~50 at a V_{DD} of 5 V and also shows a low power consumption of less than 50 nW mainly due to the presence of a reverse-biased Schottky diode. In addition, our inverter effectively operates as a photoinverter, detecting visible photons, since MoS_2 FETs appear very photosensitive, while the serially connected ZnO nanowire Schottky diode was blind to visible light. The PPC issue in the MoS_2 FET was resolved by using a small positive pulse at the gate terminal soon after light exposure. We conclude that our 1D−2D hybrid photoinverter is quite promising for both logic and photosensing inverters with high device performances.

METHODS

To fabricate the hybrid inverter, we coupled a ZnO nanowire Schottky diode with a MoS_2 nanoflake FET. A p^+-Si/SiO_2 wafer was ultrasonically cleaned in acetone, methyl alcohol, and deionized water, to be used as a substrate. On the surface of the oxygen plasma-treated substrate, the drop and dry method was used to disperse the nanowires that were in the isopropyl alcohol solution. The Ti/Au electrode was used for the good ohmic contact metal of the 200 nm thick ZnO nanowire[39] and for the bottom gate of the MoS_2 FET as well. These were patterned using the photolithography process described elsewhere.[40] A 25 nm thin Ti layer and a Au layer (Ti/Au) for the ohmic electrode were sequentially deposited on ZnO nanowires using a dc-magnetron sputtering system, which was followed by a lift-off process. For the lift-off process, acetone and lift-off layer (LOL) remover solvents were used. The same process was carried out to form Schottky contacts of e-beam deposited 100 nm thick Ni on the ZnO nanowire. Then, in order to passivate the ZnO nanowire Schottky diode and simultaneously to fabricate a dielectric layer for the MoS_2 nanoflake FET, we deposited 30 nm thin ALD Al_2O_3 on the whole device area. Using polydimethylsiloxane (PDMS) stamps, we now transferred the MoS_2 nanoflake on the bottom-gate ALD Al_2O_3 dielectric, so that our MoS_2 flake might also be aligned on the Ti/Au back-gate electrode, which was already patterned beneath Al_2O_3. We named this transfer process as nanotransfer printing, of which more details can be found in our recent report.[41]

Figure 1a−d show the nanotransfer printing processes that include flake exfoliation, gate metal locating, aligning, and printing on the gate metal. Instead of Scotch tape, PDMS stamps were used to exfoliate the MoS_2 flakes, as shown in Figure 1a. After exfoliation, many flakes were carried on the glass support, as attached on the PDMS. Among the flakes, an optimally thin flake was chosen by an optical microscope (see Figure 1b), although the optical microscope search usually selected a little thicker MoS_2 ranging from ~10 to ~80 nm in thickness. Then the optimum flake on the PDMS sample was aligned above a 30 nm thin Al_2O_3 dielectric/gate electrode by using an optical microscope and CCD camera-equipped microaligner, as shown in Figure 1c, where four arrows indicate stage translation directions for device alignment. The MoS_2 layer was aligned above the patterned bottom gate (which is the target place near the ZnO nanowire diode) and then attached by imprinting (suppressing the stage) as shown by the red arrow in Figure 1c. The upper part of Figure 1d shows the result of such nanotransfer printing; a schematic structure of the MoS_2−Al_2O_3 dielectric−Ti/Au gate is shown along with Ni−ZnO nanowire

Schottky diode. Finally, 100 nm thick Ti/Au source/drain ohmic contacts were formed on the MoS_2 flake by using a similar lift-off process to that implemented to one side of the ZnO nanowire Schottky diode, to finalize the whole device process (see the lower part of Figure 1d).

Inverter formation was simply realized by connecting the Ti/Au drain contact of the MoS_2 nanoflake FET to the Ni Schottky contact of the ZnO diode; the final electrical connection was realized by wire bonding. Figure 2a shows the schematic cross section of the inverter coupling the bottom-gate MoS_2 nanoflake FET and the ZnO nanowire source/drain, while the top-view microscopy images (optical and high-resolution scanning electron microscopies (HRSEM)) are presented in Figure 2b and c, where an inverter circuit drawing is overlaid. The channel length, L, of the MoS_2 FET was 3 μm, while our ZnO nanowire diameter was ~200 nm and the length was around 30 μm, which allowed us to fabricate an array of diodes in each substrate. All device characterizations were performed in the dark at room temperature using a semiconductor parameter analyzer (HP4155C, Agilent Technologies), and a function generator (AFG 310, Tektronix) was used for dynamic measurements on the MoS_2 nanoflake FETs.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Transfer curve, output curve, and thickness measurment of 25 nm thin MoS_2 nanoflake FET, table of information including thickness, mobility, W/L ratio, $I_{on/off}$, I_{on}, and V_D, and photoinverter dynamics under green and blue LED illumination without gate pulse. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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